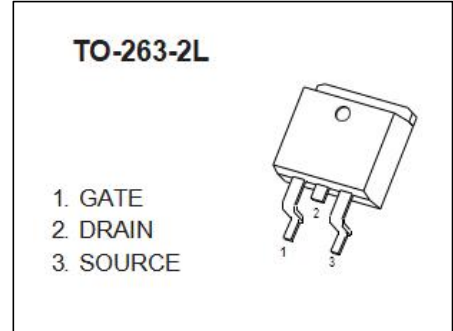




TO-263-2L Plastic-Encapsulate MOSFETS

CCMA120N10S N-Channel Power MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D
100V	4.2mΩ	120A



DESCRIPTION

The CCMA120N10S uses advanced SGT technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

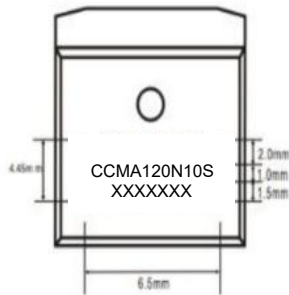
FEATURE

- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g \times R_{DS(on)}$ product(FOM)
- AEC Q101 qualified

APPLICATION

- Motor control and drive
- Battery management
- UPS (Uninterruptible Power Supplies)

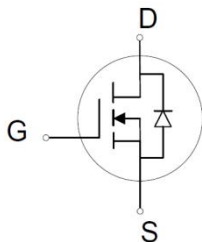
MARKING



CCMA120N10S =Part No.

XXXXXXX = Code

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS(TC=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	100	V
Gate-Source Voltage	VGS	±20	V
Continuous Drain Current ¹	ID	120	A
Pulsed Drain Current ²	IDM	480	A
Single Pulse AvalancheEnergy ³	EAS	729	mJ
Total Power Dissipation	PD	188	W
Thermal Resistance from Junction to Case	R _{θJC}	0.79	°C/W
Operating Junction and Storage Temperature Range	TJ,TSTG	-55~+175	°C
Soldering Temperature , for 10S(1.6mm from case)	-	260	°C

Notes:

1.Current is limited by package; with a Rthjc = 0.79 °C/W the chip is able to carry 141 A at 25°C.

2.Repetitive Rating: Pulse width limited by maximum junction temperature.

3.EAS condition : Tj=25°C,L=0.5mH,VGS=10V,VDD=50V, ID=54A.

MOSFET ELECTRICAL CHARACTERISTICS

TC=25°C unless otherwise specified

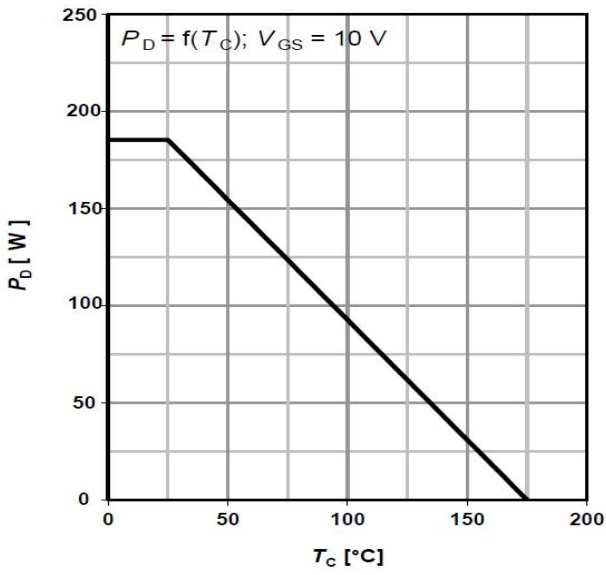
Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Off characteristics						
Drain-Source breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Gate-body leakage current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			100	nA
On characteristics						
Gate threshold voltage ³	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	3.0	4.0	V
Drain-source on-resistance ³	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		4.2	5.6	m Ω
Transconductance	g_{fs}	$V_{DS}=10\text{ V}, I_D=100\text{ A}$		204		S
Dynamic characteristics¹						
Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		4650	6050	pF
Output Capacitance	C_{oss}			2150	2800	
Reverse Transfer Capacitance	C_{rss}			160	220	
Gate resistance	R_g	$V_{GS} = 0\text{ V}, V_{DS}=0\text{ V}, f=1\text{ MHz}$		1.7		Ω
Switching characteristics¹						
Total Gate Charge	Q_g	$V_{DD} = 50\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 100\text{ A}, f = 1\text{ MHz}$		113		nC
Gate-Source Charge	Q_{gs}			38		
Gate-Drain Charge	Q_{gd}			23		
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, V_{GS} = 10\text{ V},$ $I_D = 100\text{ A}, R_G = 3.5\ \Omega$		25		ns
Turn-on rise time	t_r			15		
Turn-off delay time	$t_{d(off)}$			53		
Turn-off fall time	t_f			18		
Drain-Source Diode Characteristics						
Drain-source diode forward Voltage ³	V_{SD}	$V_{GS} = 0\text{ V}, I_{SD} = 100\text{ A}, T_j = 25\text{ }^\circ\text{C}$			1.2	V
Continuous drain-source diode forward current ²⁴	I_S	$T_C = 25\text{ }^\circ\text{C}$			120	A
Pulsed drain-source diode forward current	I_{SM}				480	A
Reverse recovery time	t_{rr}	$I_F=100\text{ A}, dI/dt=100\text{ A/us}$		75		ns
Reverse recovery charge	Q_{rr}				163	

Notes :

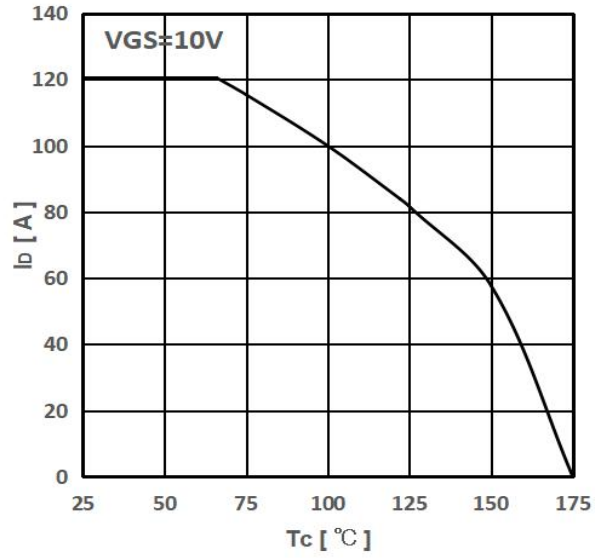
1. Guaranteed by design, not subject to production.
2. Surface Mounted on FR4 Board, $t \leq 10\text{ sec}$.
3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Current is limited by package; with a $R_{thjc} = 0.79\text{ }^\circ\text{C/W}$ the chip is able to carry 141 A at 25°C.

Typical Characteristics

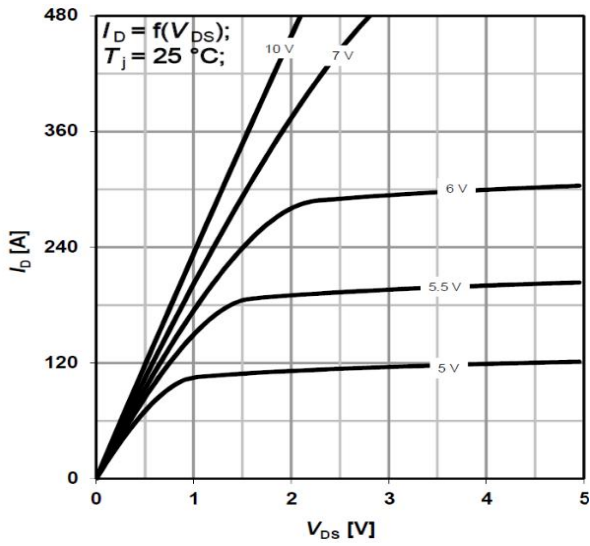
PD -- Tc



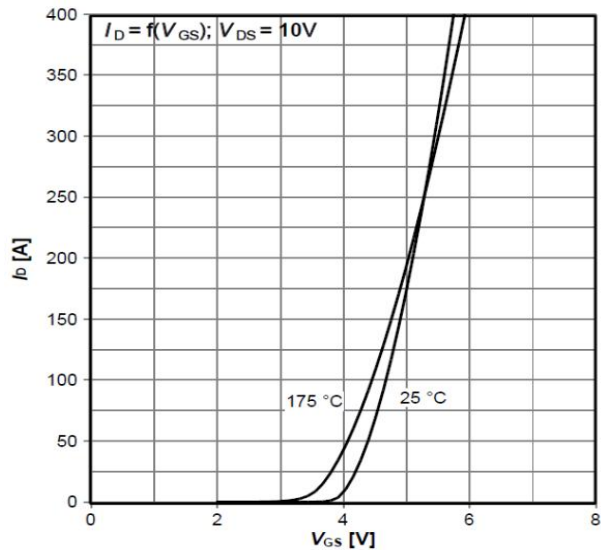
ID -- Tc



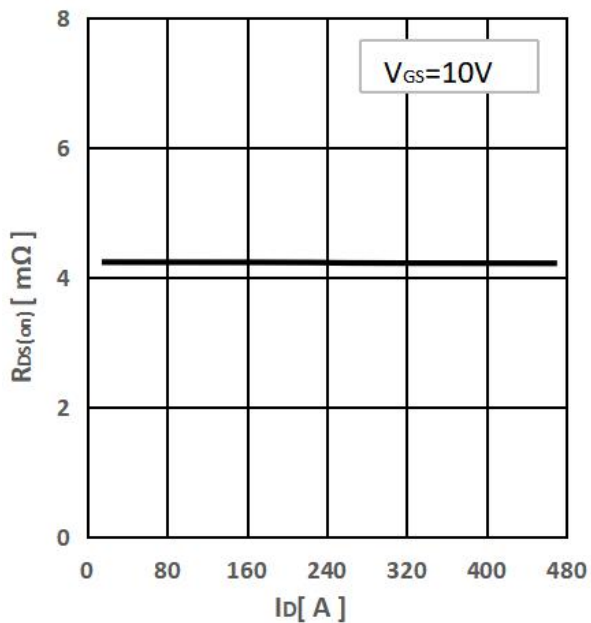
ID -- VDS



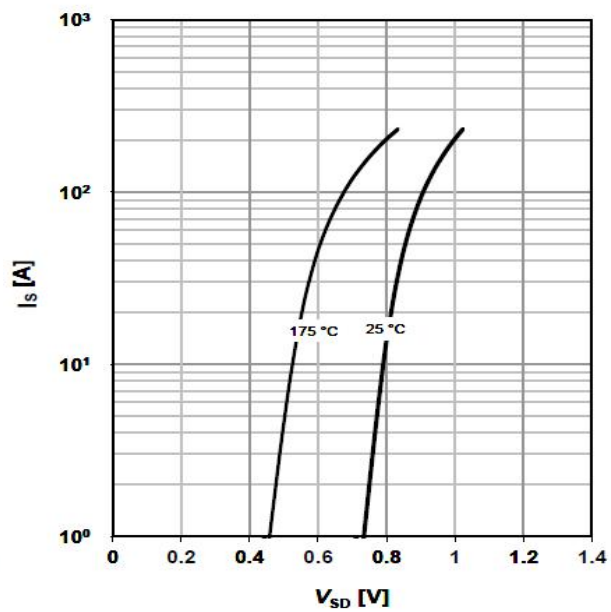
ID -- VGS



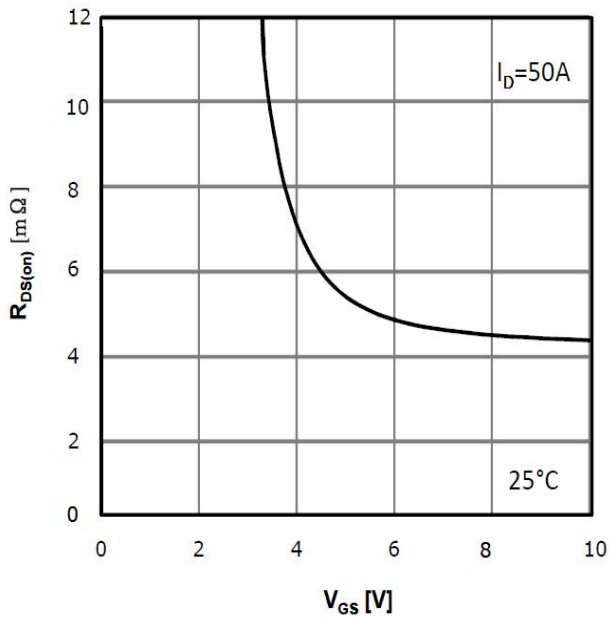
RDS(on) -- ID



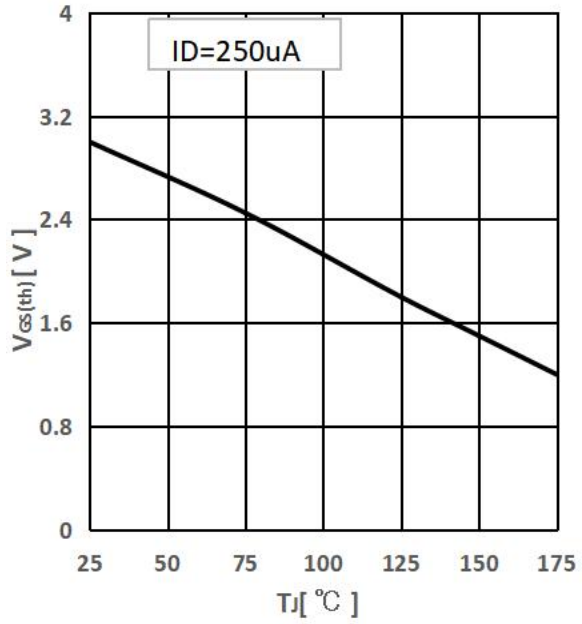
IS -- VSD



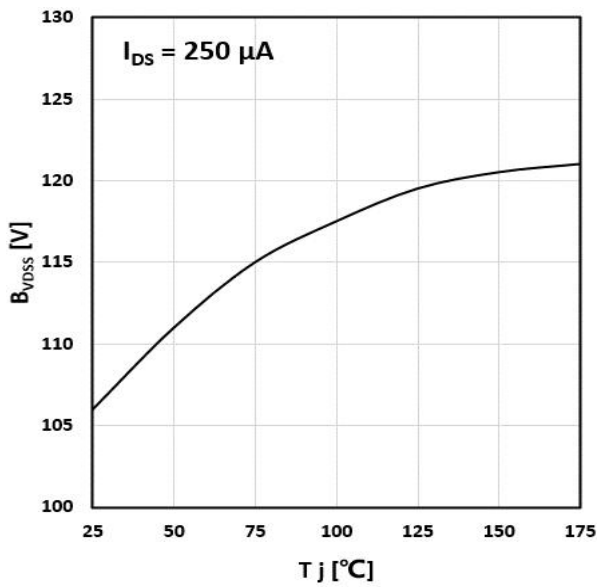
RDS(on) -- VGS



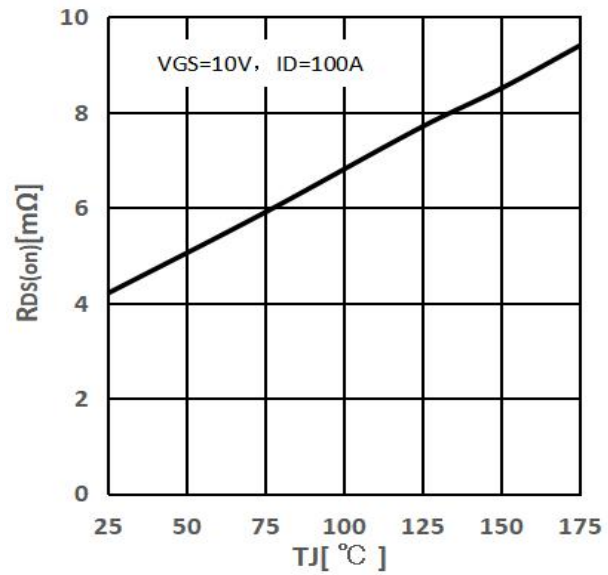
Threshold Voltage



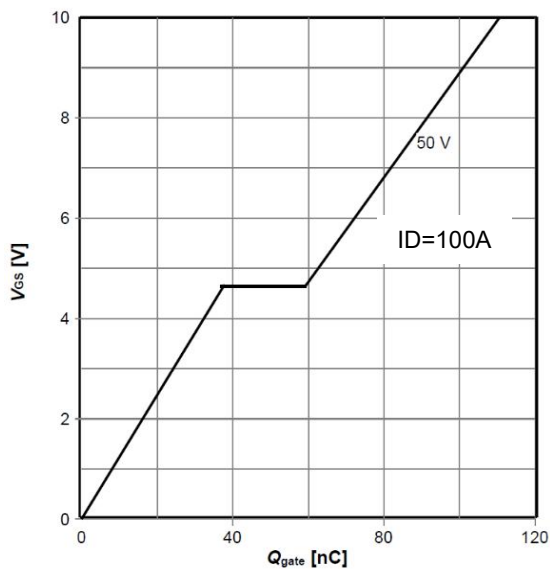
Drain-source breakdown voltage



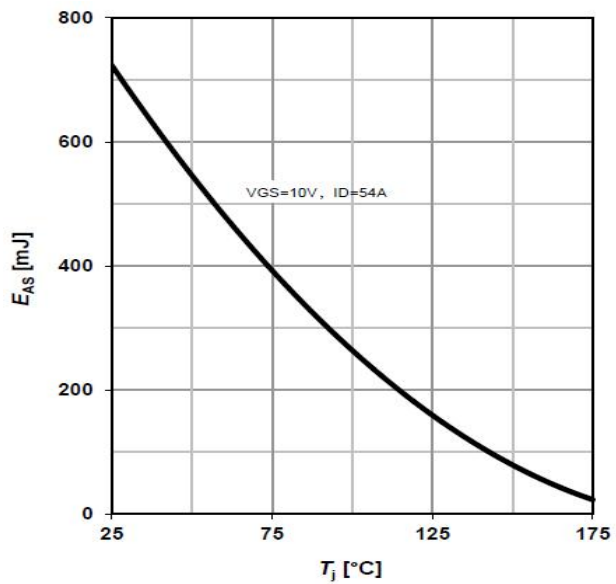
RDS (on) -- Tj



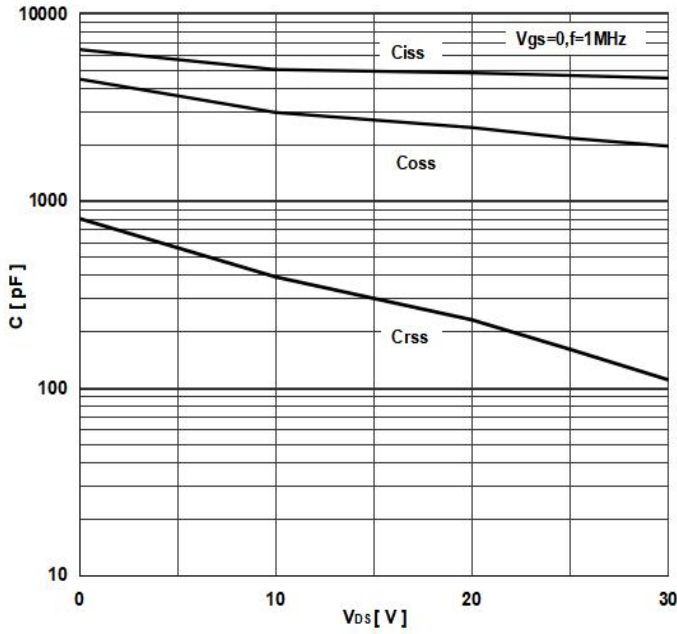
Typ.gate charge



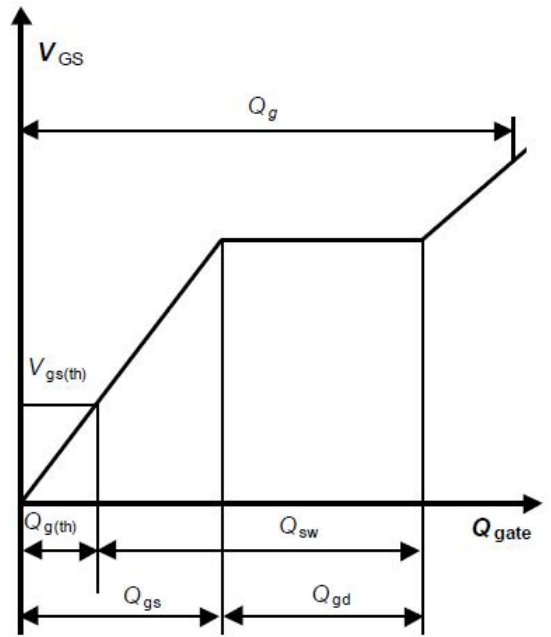
Avalanche energy



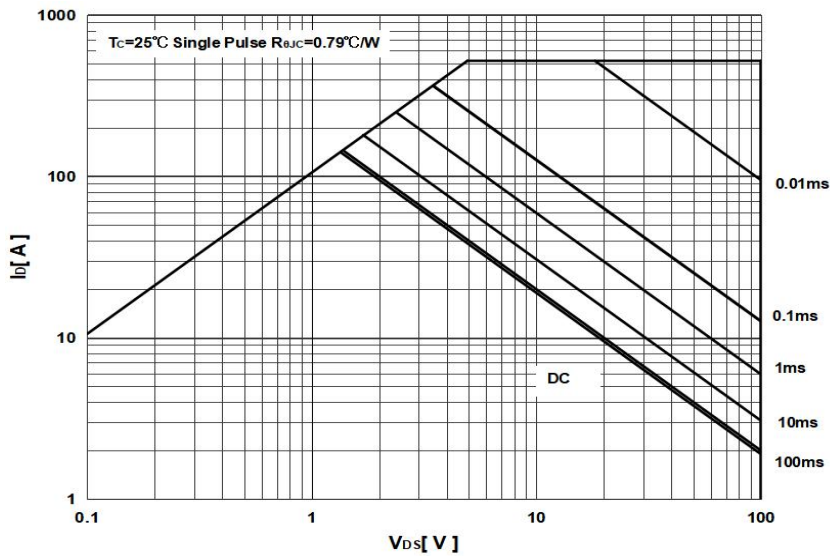
Typ. capacitance



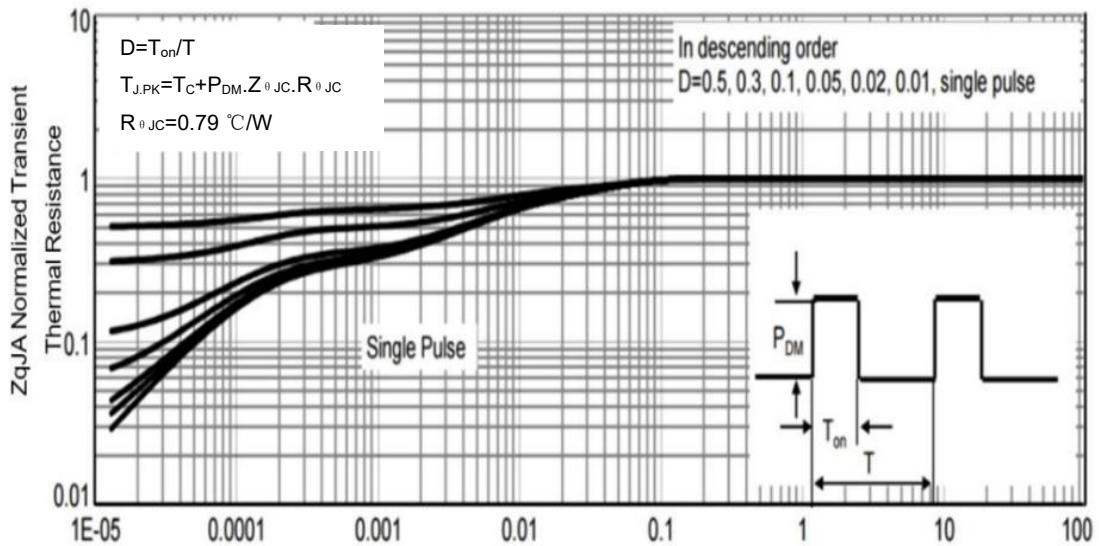
Gate charge waveforms



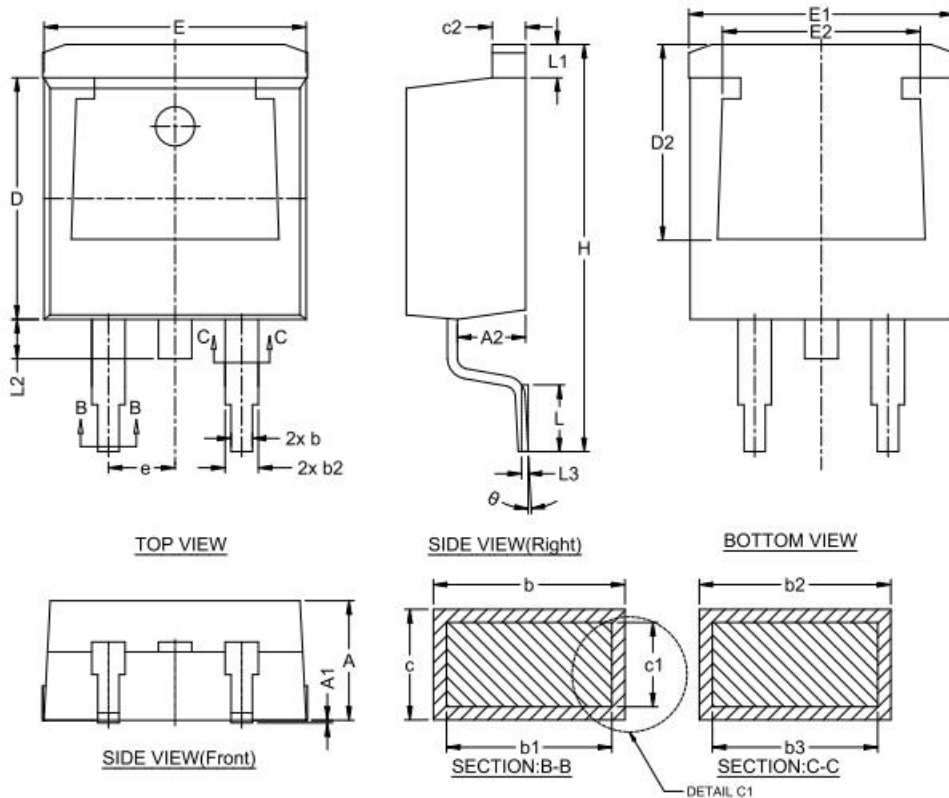
Safe operating area



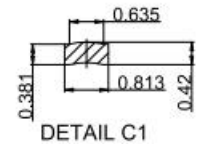
Normalized Thermal Transient Impedance



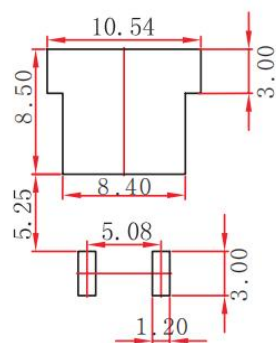
TO-263-2L Package Outline Dimensions



DIM SYMBOL	MIN.	NOM.	MAX.
A	4.450	4.550	4.650
A1	0.000	---	0.150
A2	2.500	2.600	2.700
b	0.753	0.853	0.953
b1	0.713	0.813	0.913
b2	1.210	1.310	1.410
b3	1.170	1.270	1.370
c	0.330	0.421	0.521
c1	0.281	0.381	0.481
c2	1.210	1.310	1.410
D	9.100	9.200	9.300
D2	7.215	7.415	7.615
E	9.900	10.000	10.100
E1	9.900	10.100	10.300
E2	7.341	7.541	7.741
e	2.540 BSC.		
H	15.300	15.500	15.700
L	2.340	2.540	2.740
L1	1.066	1.266	1.466
L2	1.400	1.500	1.600
L3	0.254 BSC.		
θ	0°	---	5°



TO-263-2L Suggested Pad Layout



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: 0.5mm.
3. The pad layout is for reference purposes only.

NOTICE

Cloudchild reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to any product herein. Cloudchild does not assume any liability arising out of the application or use of any product described herein.

ChongQing Cloudchild Technology Co., Ltd. (short for Cloudchild) exerts the greatest possible effort to ensure high quality and reliability. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing Cloudchild products, to comply with the standards of safety in making a safe design for the entire system, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue. In developing your designs, please ensure that Cloudchild products are used within specified operating ranges as set forth in the most recent Cloudchild products specifications.

Date of change	Rev #	revise content
2024/01/20	A/0	/